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PATENT
ATTY. DOCKET NO. IBM/67DV1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Galbraith et al. Art Unit: 2187
Serial No. : 09/935,939 Examiner: Brian Peugh
Filed : August 23, 2001
For : ADVANCED READ CACHE MANAGEMENT

Assistant Commissioner of Patents
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Washington, DC 20231

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MAY 02 2003

AMENDMENT FOR APPEAL

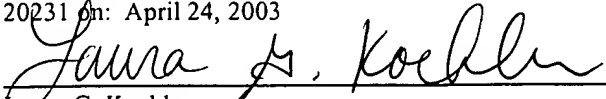
Technology Center 2100

Clean Version of Amendments

51. The cache control circuit of claim 50 wherein said control circuit maintains statistics on types of accesses made to data by maintaining a counter associated with blocks of data, said counters being credited or penalized in response to types of accesses made to the associated block of data.

52. The cache control circuit of claim 51 wherein said control circuit maintains statistics by crediting a counter by a predetermined credit in response to a read to a block of data associated with said counter, and penalizing said counter by a

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid in an envelope addressed to: Assistant Commissioner of Patents, Box AF FEE, Washington, D.C. 20231 on: April 24, 2003


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